REMARKS

Claims 1 through 9 and 11 through 39 are pending in the application.

Objections to the Drawings

The drawings were objected to under 37 C.F.R. § 1.83(a). In particular, the drawings were objected to as not showing a feature of the claims, namely "an importance level of the line after the valid data is accessed while maintaining the line as a valid line." Applicant respectfully requests reconsideration of this objection. Looking at Fig. 3, a number of cache lines is shown. In the column preceding column 37, cache line 0 is the least recently used (LRU) cache line followed in order by cache lines 2, 3 and 1. Thus, cache line 1 is the most recently used (MRU) cache line of the four. Cache line 1 contains a copy of the data for main memory location b as indicated in the drawing figure and at page 7, lines 2-3 of the specification. In column 37, an RICL (reduced importance cache line) instruction is executed. This instruction has the effect of changing the importance level of cache line 1 from the most recently used to the least recently used. In column 38, a memory access is made. As shown in the drawing figure (bottom of column 38) and at page 7, lines 4-14, the data for b is replaced.

Throughout the figure, each cache line contains data to be accessed by the CPU. Note that in the third column of the figure, the data for main memory location is loaded into cache line 1 (see "Allocation b==>1"). The memory access of the column before column 37 is for valid data for memory location b. Such is implicit from the drawing figure since no allocation is shown in this column. Thus, the feature of reducing an importance level of the line after the valid data is accessed while maintaining the line as a valid line is shown in the drawing figures. Accordingly, reconsideration and withdrawal of the objection to the drawing figures is respectfully requested.

Rejections of the Claims under 35 U.S.C. § 112, First Paragraph

Claims 1-39 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. In particular, the Office Action points to the language of "reducing an importance level of the line after the valid data is accessed while maintaining the line as a valid line." The Office Action states that the "Examiner is unclear as to the meaning of

this claim limitation." As presented in the previous Amendment, the cited art describes invalidating cache lines, while in embodiments of the present invention, a cache line remains valid, but its importance level has been changed.

As described above, in the third column of Fig. 3, the data for memory location b is loaded into cache line 1. This is shown diagrammatically in Fig. 3 in the second row (row Q) where the Allocation is reflected as "b==>1." As seen from Fig. 3, cache line 1 becomes the most recently used cache line and is moved to the highest level of importance, row U. In the column preceding column 37, the CPU accesses the data from memory location b from cache line 1. This is valid cache data, and cache line 1 is moved to the most recently used importance level (row U). The RICL instruction changes the importance level of cache line 1 to least recently used (row R). The contents of the cache lines 0-3 are the same for column 37 and the two columns preceding it. Thus, cache line 1 included valid data in the column preceding column 37 and includes valid data in column 37 as well. Since its importance level has been reduced, cache line 1 is selected for replacement and in column 39, the data from memory location b is replaced with data from memory location e.

As indicated at page 7, lines 11-14, reducing the importance level of cache line 1, allows other cache lines that would otherwise be at the lowest importance level to be available for future accesses. As seen in Fig. 3, without the RICL instruction, data from memory location c stored in cache line 2 would have been replaced with data from memory location e. In the column immediately after column 38, the access to data from memory location a would result in a "cache miss" and the resulting delays associated with it.

As seen from Fig. 3, the data in cache lines 0-3 is valid data available for access by the CPU. Using the presently claimed invention provides changing the relative importance level for these cache lines while maintaining valid data in them. Such is clearly shown in the specification (e.g., page 6, line 26 to page 7, line 14) and the drawings (e.g., Fig. 3). Accordingly, reconsideration and withdrawal of the rejection of claims 1-39 under 35 U.S.C. § 112, first paragraph is respectfully requested.

CONCLUSION

In view of the above remarks, the Applicant respectfully submits that the present case is in condition for allowance and respectfully requests that the Examiner issue a notice of allowance for all currently pending claims.

The Office is hereby authorized to charge any fees determined to be necessary under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Kenyon & Kenyon **Deposit Account No. 11-0600**.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application.

Respectfully submitted,

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